Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.An apparatus for generating a phase delay, comprising:

a buffer for buffering an input signal and outputting an output signal;

a DAC for outputting a control voltage corresponding to a digital value representative of a phase delay; and

a variable capacitor coupled to the DAC and the buffer, the capacitance value of the variable capacitor corresponding to the control voltage;

wherein by controlling the capacitance value, the apparatus adjusts the phase delay between the input signal and the output signal.

[c2] 2.The apparatus of claim 1, wherein the input signal is a clock signal.

[c3] 3.The apparatus of claim 1, wherein the input signal is a RF signal.

[c4] 4.The apparatus of claim 1, wherein the variable capacitor is a voltage-controlled capacitor.

[c5] 5.The apparatus of claim 4, wherein the voltage-controlled capacitor is a MOS-based voltage-controlled capacitor.

[c6] 6.The apparatus of claim 4, wherein the voltage-controlled capacitor is a P+/N well junction voltage-controlled capacitor.

[c7] 7.A method for generating a phase delay comprising the following steps:
buffering an input signal to generate an output signal;
providing a digital value representative of a phase delay;
generating a control voltage corresponding to the digital value representative of the phase delay; and
adjusting a capacitance value of a variable capacitor with the control voltage, to adjust the phase delay between the input signal and the output signal.

[c8] 8.The method of claim 7, wherein the input signal is a clock signal.

[c9] 9.The method of claim 7, wherein the input signal is a RF signal.

[c10] 10.The method of claim 7, wherein the control voltage generating step is implemented by a DAC.

[c11] 11.The method of claim 7, wherein the variable capacitor

is a voltage-controlled capacitor.

[c12] 12.The method of claim 11, wherein the voltage-controlled capacitor is a MOS-based voltage-controlled capacitor.

[c13] 13.The method of claim 11, wherein the voltage-controlled capacitor is a P+/N well junction voltage-controlled capacitor.